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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/803,334	03/09/2001	David Homol	4015-826	7343

24112 7590 07/02/2004

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EXAMINER	
LIU, SHUWANG	
ART UNIT	**PAPER NUMBER**
2634	4

DATE MAILED: 07/02/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/803,334	HOMOL ET AL.	
	Examiner	Art Unit	
	Shuwang Liu	2634	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 March 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4,7,8,11,14,15,17,19,22 and 23* is/are rejected.

7)☒ Claim(s) *3,5,6,9,10,12,13,16,18,20,21 and 24* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2 and 3*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

2. Claims 1, 2, 4, 7, 8, 11, 14, 15, 19, 22 and 23 are rejected under 35 U.S.C. 102(a) as being anticipated by Klemmer et al. (US 6,265,902).

As shown in figures 1-3, Klemmer et al. discloses:

(1) regarding claim 1:

a circuit for use in a phase-locked loop (PLL) comprising:

a phase detector (310) comprising:

first (400) and second (402) input circuits to generate first and second PLL control signals responsive to clock edges in first and second input signals, respectively; and

a reset circuit (404) to generate a reset signal based on said first and second PLL control signals to reset said first and second input circuits (column 8, lines 52-67); and

a cycle slip detector (315 and 320) for each one of said first and second input circuits, each said cycle slip detector generating a slip indication signal based on said reset signal, a corresponding one of said first and second input signals, and a corresponding one of said first and second PLL control signals (column 7, line 24-

column 12, line 63).

(2) regarding claim 2:

wherein each the cycle slip detector comprises slip detection logic (for example, 408, 410 and 406) to generate slip indication signal (for example, 375) when a clock edge in the corresponding one of the first and second input signals is received during the reset signal (column 7, line 24-column 12, line 63).

(3) regarding claim 4:

wherein each the cycle slip detector comprises slip detection logic (for example, 408, 410 and 406) to generate slip indication signal (for example, 375) when a clock edge in the corresponding one of the first and second input signals is received when the corresponding one the first and second PLL control signals is asserted (column 7, line 24-column 12, line 63).

(4) regarding claim 7:

wherein each said first and second input circuits comprises a latching circuit (400 and 402) generating a corresponding one of said first and second PLL control signals as a latched output signal responsive to a first clock edge in a corresponding one of said first and second input signals.

(5) regarding claim 8:

wherein said latching circuit comprises a reset input coupled to said reset signal and operative to reset said latched output signal when said reset signal is asserted so that said latching circuit responds to a next clock edge in said corresponding one of said first and second input signals (column 8, lines 53-67).

(6) regarding claim 11:

A phase-locked loop (PLL) comprising:

a phase detector (310) to generate first and second PLL control signals based on a detected phase difference between respective clock edges in first and second input signals (335 and 340), said phase detector comprising:

first and second input circuits (400 and 402) to generate first and second PLL control signals responsive to clock edges in first and second input signals, respectively; and

a reset circuit (404) to generate a reset signal based on said first and second PLL control signals to reset said first and second input circuits; and

a control circuit (525) to generate a control signal based on said first and second PLL control signals;

a controllable oscillator (535) to generate an output signal at a frequency based on said control signal; and

a first cycle slip detector (315) to generate a first cycle slip indicator signal when a clock edge in said first input signal occurs during said reset signal; and

a second cycle slip detector (320) to generate a second cycle slip indicator when a clock edge in said second input signal occurs during said reset signal;

wherein said first input signal is derived from a reference clock signal and said second input signal is derived from a frequency-controlled output of said PLL (column 7, line 24-column 12, line 63).

(7) regarding claim 14:

wherein each said first and second input circuits comprises a latching circuit (400 and 402) generating a corresponding one of said first and second PLL control signals as a latched output signal responsive to a first clock edge in a corresponding one of said first and second input signals.

(8) regarding claim 15:

wherein said latching circuit comprises a reset input coupled to said reset signal and operative to reset said latched output signal when said reset signal is asserted so that said latching circuit responds to a next clock edge in said corresponding one of said first and second input signals (column 8, lines 53-67).

(9) regarding claim 19:

a method of detecting cycle slip in a phase detector circuit, the method comprising:

operating said phase detector (310) to generate first and second PLL control signals (350 and 355) based on latching respective first clock edges in first and second input signals (335 and 340);

resetting (404) said phase detector with a reset pulse after both said first clock edges occur to make said phase detector responsive to next clock edges in said first and second input signals;

generating a slip indicator signal (375 and 380)) in response to said next clock edge occurring in at least one of said first and second input signals before said reset pulse, and in response to any clock edge in at least one of said first and second input signals occurring during said reset pulse (column 7, line 24-column 12, line 63).

(10) regarding claim 22:

further comprising determining whether a missed clock edge is an up-cycle slip or a down-cycle slip based on determining whether said phase detector misses a clock edge in said first input signal or in said second input signal, respectively (column 7, line 24-column 12, line 63).

(11) regarding claim 23:

further comprising generating said cycle slip indicator signal (UP and DOWN) as an up-cycle slip indicator (UP) upon occurrence of said up-cycle slip and generating said cycle slip indicator signal as a down-cycle slip indicator (DOWN) upon occurrence of said down-cycle slip.

Double Patenting

3. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

4. Claims 1, 11, 17 and 19 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 21, 29, 31 and 37 of patent No. 6,441,691. Although the conflicting claims are not identical, they are not patentably distinct from each other because the broader application claims would have been obvious in view of the narrow issued claims (see In re Emert, 124 F.3d 1458, 44 USPQ2d 1149).

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Allowable Subject Matter

5. Claims 3, 5, 6, 9, 10, 12, 13, 16-18, 20, 21 and 24 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

6. The following is a statement of reasons for the indication of allowable subject matter: the prior art does not teach or fairly suggest a circuit slip detection logic comprises a delay element to generate a delayed version of said reset signal, and wherein said slip detection logic additionally generates said slip indication signal in response to receiving a clock edge in said corresponding one of said first and second input signals when said delayed version of said reset signal is asserted.

Conclusion

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shuwang Liu whose telephone number is (703) 308-9556.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Stephen Chin, can be reached at (703) 305-4714.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to:

(703) 872-9306 (for Technology Center 2600 only)

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Sixth Floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office whose telephone number is (703) 306-0377.

Shuwang Liu
Primary Examiner
Art Unit 2634

June 25, 2004